What is claimed is:

1. A method of fabricating a metal-insulator-metal (MIM) capacitor structure in an integrated circuit, the method comprising:

(a) fabricating first and second legs of MIM capacitor structure in an integrated circuit, the first and second legs extending generally parallel to one another and defining a channel therebetween, each leg including top and bottom electrodes, an insulator layer interposed between the top and bottom electrodes, and a sidewall that faces the channel; and

(b) fabricating a sidewall spacer extending along the channel, the sidewall spacer including a conductive layer and a dielectric layer interposed between the conductive layer and the sidewall of the first leg, wherein the conductive layer of the sidewall spacer is physically separated from the top electrode.

2. The method of claim 1, wherein fabricating the first and second legs includes fabricating the bottom electrode for the first leg by depositing titanium nitride.

3. The method of claim 2, wherein fabricating the bottom electrode for the first leg includes:

(a) fabricating an interconnect layer upon which the titanium nitride is deposited; and

(b) patterning the interconnect layer and titanium nitride to define the bottom electrode.

4. The method of claim 3, wherein fabricating the bottom electrode for the first leg further comprises ammonia plasma treating a surface of the titanium nitride to improve the surface barrier characteristic to oxygen.

5. The method of claim 1, wherein fabricating the first and second legs includes fabricating the insulator layer for the first leg, including depositing high dielectric constant material over the bottom electrode of the first leg.

6. The method of claim 5, further comprising annealing the bottom electrode for the first leg prior to fabricating the insulator layer for the first leg.

7. The method of claim 6, wherein fabricating the sidewall spacer comprises depositing high dielectric constant material over the sidewall of the first leg.

8. The method of claim 7, wherein depositing the high dielectric constant material over the bottom electrode of the first leg, and depositing the high dielectric constant material over the sidewall of the first leg, are performed concurrently.

9. The method of claim 8, wherein the high dielectric constant material deposited over the bottom electrode and sidewall of the first leg comprises tantalum pentoxide.

10. The method of claim 8, wherein fabricating the first and second legs further includes fabricating the top electrode for the first leg by depositing a conductive material over the insulator layer of the first leg, and wherein fabricating the sidewall spacer comprises fabricating the conductive layer for the sidewall spacer by depositing a conductive material over the dielectric layer for the sidewall spacer concurrently with depositing the conductive material over the insulator layer of the first leg.

11. The method of claim 10, wherein fabricating the first and second legs further includes patterning the top electrode and insulator layers of the first leg, and wherein fabricating the sidewall spacer includes physically separating a portion of the conductive layer in the channel from the top electrode of the first leg.

12. The method of claim 11, wherein patterning the top electrode and insulator layers of the first leg, and physically separating the portion of the conductive layer in the channel are concurrently performed via an anisotropic etching operation.

13. The method of claim 12, wherein the anisotropic etching operation includes:

(a) patterning a resist layer that covers the first leg to define the top electrode of the first leg;

(b) etching through the resist layer at a first rate until reaching a first point proximate an interface between the top electrode the insulator layer of the first leg; and

(c) etching through the resist layer at a second rate that is slower than the first rate until reaching a second point proximate the bottom electrode of the first leg.

14. The method of claim 13, wherein the bottom electrode includes an etch stop layer, wherein etching through the resist layer at the second rate is performed until reaching a second point proximate the etch stop layer.

15. The method of claim 7, wherein depositing the high dielectric constant material over the bottom electrode of the first leg, and depositing the high dielectric constant material over the sidewall of the first leg, are performed using metal organic chemical vapor deposition (MOCVD).

16. The method of claim 1, wherein the MIM capacitor structure includes a serpentine pattern including a plurality of legs arranged in a generally parallel relationship.

17. The method of claim 1, wherein the serpentine pattern comprises a positive serpentine pattern.

18. The method of claim 1, wherein the serpentine pattern comprises a negative serpentine pattern.

19. The method of claim 18, wherein the serpentine pattern additionally comprises a positive serpentine pattern, wherein the positive and negative serpentine patterns are interleaved.

20. A metal-insulator-metal (MIM) capacitor structure for use in an integrated circuit, the MIM capacitor structure comprising:

(a) first and second legs extending generally parallel to one another and defining a channel therebetween, each leg including top and bottom electrodes, an insulator layer interposed between the top and bottom electrodes, and a sidewall that faces the channel; and

(b) a sidewall spacer extending along the channel, the sidewall spacer including a conductive layer and a dielectric insulator layer interposed between the conductive layer and the sidewall of the first leg, wherein the conductive layer of the sidewall spacer is physically separated from the top electrode.

21. The MIM capacitor structure of claim 20, wherein the bottom electrode for the first leg comprises titanium nitride.

22. The MIM capacitor structure of claim 21, wherein the bottom electrode for the first leg further includes an interconnect layer upon which the titanium nitride is deposited.

23. The MIM capacitor structure of claim 22, wherein the titanium nitride includes an ammonia plasma treated surface.

24. The MIM capacitor structure of claim 21, wherein the insulator layer for the first leg, and the dielectric layer in the sidewall spacer, each comprise a high dielectric constant material.

25. The MIM capacitor structure of claim 24, wherein the high dielectric constant material in the insulator layer for the first leg and the dielectric layer in the sidewall spacer is tantalum pentoxide.

26. The MIM capacitor structure of claim 24, wherein the top electrode for the first leg includes titanium nitride.

27. The MIM capacitor structure of claim 20, wherein the first and second legs are defined within a serpentine pattern.

28. The MIM capacitor structure of claim 20, wherein the serpentine pattern comprises at least one of a positive serpentine pattern and a negative serpentine pattern.

29. The MIM capacitor structure of claim 28, wherein the serpentine pattern comprises a positive serpentine pattern interleaved with a negative serpentine pattern.

30. A method of fabricating a metal-insulator-metal (MIM) capacitor structure in an integrated circuit, the method comprising:

(a) forming first and second bottom electrodes in an integrated circuit, the first and second electrodes extending generally parallel to one another and defining a channel therebetween;

(b) depositing an insulator layer over the first and second bottom electrodes and in the channel;

(c) depositing a conductive layer over the insulator layer; and

(d) etching the deposited conductive and insulator layers to define first and second top electrodes opposing the first and second bottom electrodes, and to physically separate a portion of the conductive layer in the channel.

31. The method of claim 30, wherein forming the first and second bottom electrodes comprises:

(a) forming an interconnect layer in the integrated circuit;

(b) depositing an anti-reflective coating (ARC) layer over the interconnect layer; and

(c) concurrently patterning the interconnect and ARC layers to form the first and second bottom electrodes.

32. The method of claim 31, wherein the interconnect layer comprises aluminum, copper or a combination thereof, and wherein the ARC layer comprises titanium nitride.

33. The method of claim 32, wherein depositing the insulator layer over the first and second bottom electrodes and in the channel comprises depositing tantalum pentoxide.

34. The method of claim 33, further comprising ammonia plasma treating the ARC layer prior to depositing the insulator layer.

35. The method of claim 34, further comprising annealing the first and second bottom electrodes prior to depositing the insulator layer.

36. The method of claim 30, wherein etching the deposited conductive and insulator layers comprises etching the deposited conductive and insulator layers anisotropically.

37. The method of claim 36, wherein etching the deposited conductive and insulator layers includes:

(a) patterning a resist layer;

(b) etching through the resist layer at a first rate until reaching a first point proximate an interface between the conductive and insulator layers; and

(c) etching through the resist layer at a second rate that is slower than the first rate until reaching a second point proximate the first and second bottom electrodes.

38. The method of claim 37, wherein through the resist layer at the first rate includes etching at the first rate for a first period of time, and wherein etching through the resist layer at the second rate includes:

(a) etching at the second rate until detecting an endpoint associated with the interface between the conductive and insulator layers; and

(b) thereafter etching at the second rate for a second period of time.

39. A method of fabricating a metal-insulator-metal (MIM) capacitor structure in an integrated circuit, the method comprising ammonia plasma treating a surface of a bottom electrode of the MIM capacitor structure prior to depositing an insulator layer over the bottom electrode to improve the surface barrier characteristic to oxygen.

40. The method of claim 39, wherein the bottom electrode comprises titanium nitride disposed at the surface of the bottom electrode.

41. The method of claim 40, wherein the insulator layer comprises tantalum pentoxide.

42. The method of claim 40, wherein ammonia plasma treating comprises bombarding the titanium nitride surface with nitrogen ions to inhibit oxidation of the titanium nitride surface.

43. The method of claim 40, wherein ammonia plasma treating is performed in a plasma enhanced chemical vapor deposition tool.

44. The method of claim 43, wherein ammonia plasma treating is performed in an atmosphere comprising ammonia and an inert gas.

45. The method of claim 44, wherein ammonia plasma treating is performed in an atmosphere having a pressure of about 10 milliTorr to about 10 Torr and a bottom electrode temperature of about 300 to about 500 °C.

46. The method of claim 43, wherein ammonia plasma treating includes applying RF power including up to about 50 % low frequency RF power.

47. A metal-insulator-metal (MIM) capacitor structure for use in an integrated circuit, the MIM capacitor structure comprising:

(a) top and bottom electrodes, wherein the bottom electrode includes an ammonia plasma treated surface; and

(b) an insulator layer interposed between the top electrode and the ammonia plasma treated surface of the bottom electrode.

48. The MIM capacitor structure of claim 47, wherein the ammonia plasma treated surface comprises titanium nitride.

49. The MIM capacitor structure of claim 48, wherein the insulator layer comprises tantalum pentoxide.

50. The MIM capacitor structure of claim 48, wherein the ammonia plasma treated surface is substantially free of titanium oxide as a result of bombardment of the ammonia plasma treated surface with nitrogen ions.

51. A method of fabricating a metal-insulator-metal (MIM) capacitor structure in an integrated circuit, the method comprising:

(a) patterning a resist layer that covers a MIM capacitor structure to define a top electrode, the MIM capacitor structure including an etch stop layer, a dielectric layer overlaying the etch stop layer, and a conductive layer overlaying the dielectric layer;

(b) etching the MIM capacitor structure through the resist layer at a first rate until reaching a first point proximate an interface between the conductive and dielectric layers; and

(c) etching the MIM capacitor structure through the resist layer at a second rate that is slower than the first rate until reaching a second point proximate the etch stop layer.

52. The method of claim 51, wherein the conductive layer and the etch stop layer each comprise titanium nitride.

53. The method of claim 52, wherein the dielectric layer comprises tantalum pentoxide.

54. The method of claim 51, wherein the etch stop layer is disposed on a bottom electrode defined for the MIM capacitor structure.

55. The method of claim 54, wherein etching the MIM capacitor structure at the first and second rates is performed using etching chemistry that includes at least one chlorine containing compound, wherein the bottom electrode further comprises aluminum, and wherein the etch stop layer is configured to prevent exposure of the aluminum in the bottom electrode to the etching chemistry.

56. The method of claim 54, wherein patterning the resist layer includes defining a pattern in the resist layer via photolithography, wherein the etch stop layer

is further configured as an anti-reflective coating for the bottom electrode to inhibit reflections when defining the pattern in the resist layer.

57. The method of claim 54, wherein the conductive layer comprises about 300 nm of titanium nitride, wherein the etch stop layer comprises about 30 nm of titanium nitride, wherein the first rate comprises about 300 to about 400 nm/minute, and wherein the second rate comprises about 50 to about 100 nm/minute.

58. The method of claim 54, wherein the bottom electrode comprises first and second legs extending generally parallel to one another and defining a channel therebetween, each leg including a sidewall that faces the channel, wherein the dielectric layer overlays the sidewall of each leg of the bottom electrode, and wherein the conductive layer overlays the dielectric layer that overlays the sidewall of each leg of the bottom electrode, and wherein etching at the first and second rates each comprise anisotropically etching such that subsequent to etching at the first and second rates a sidewall spacer extends along the channel, the sidewall spacer comprising that portion of the conductive layer and the dielectric layer that overlay the sidewall subsequent to etching at the first and second rates.

59. The method of claim 51, wherein etching the MIM capacitor structure through the resist layer at the first rate includes etching the MIM capacitor structure at the first rate for a first period of time, and wherein etching the MIM capacitor structure through the resist layer at the second rate includes:

(a) etching the MIM capacitor structure at the second rate until detecting an endpoint associated with the interface between the conductive and dielectric layers; and

(b) thereafter etching the MIM capacitor structure at the second rate for a second period of time.

60. The method of claim 59, wherein the first period of time is empirically selected to etch about 70 % of the conductive layer.

61. The method of claim 59, further comprising:

(a) tracking a third period of time until detecting the endpoint; and

(b) calculating the second period of time from the third period of time.

62. The method of claim 61, wherein calculating the second period of time includes selecting the second period of time to be about 30 % of the third period of time.